Shri Vaishnav Vidyapeeth Vishwavidyalaya, Indore (MP)

Choice Based Credit System (CBCS) Scheme

Bachelor of Technology (Electronics & Communication)

V - SEMESTER

Sr. No.	Subject Code	Name of Subject	Course Code	Teaching Scheme/ Week			Examination Scheme					Total Marks	Credits
							Theory			Practical			
				L	T	P	End Sem Unversity Exam	Two Term Exam	Teachers Asses-ment*	End Sem Unversity Exam	Teachers Asses-ment*		
1	BTEC501	Microprocessors & Interfacing		3	1	2	60	20	20	30	20	150	5
2	BTEC502	Cellular & Mobile Communication		3	1	0	60	20	20	0	0	100	4
3	BTEC503	Digital Communication		3	1	2	60	20	20	30	20	150	5
4	BTEC504	CMOS VLSI Design		3	1	2	60	20	20	30	20	150	5
5	BTEC515/ BTEC525/ BTCS403/ BTEI603	Electives: 1 Data Communication 2 FPGA Based System Design 3 Data Structures & Algorithms 4 Process Control Engineering		3	1	2	60	20	20	30	20	150	5
6	BTEC506	Minor Project		0	0	2	0	0	0	30	20	50	1
7	BTEC507	Software lab-II (Communication Systems)		0	0	2	0	0	0	30	20	50	1
TOTAL				**15**	**5**	**12**	**300**	**100**	**100**	**180**	**120**	**800**	**26**

***Teacher Assessment shall be based on following components: Quiz/Assignment/Project/Participation in Class, given that no component shall exceed more than 10 marks.**

Chairperson
Board of Studies
Shri Vaishnav Vidyapeeth Vishwavidyalaya
Indore

Registrar
Shri Vaishnav Vidyapeeth Vishwavidyalaya
INDORE (M.P.)